REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 1-18 and 23-24 are pending and rejected. Claim 1 is amended and Claim 10 is cancelled hereinabove.

The Applicants respectfully traverse the objection to the Drawings on page 3 of the Office Action. Specifically, "powering down, with a power switch, the circuitry for operating the row of memory cells preceding the intervention circuit" is element 320 of FIG. 3 (Specification page 14 lines 18-20 and page 15 lines 6-8; see also element 118 of FIG. 1a plus page 11 lines 14-17 and page 12 lines 8-9). FIG. 3 also shows the limitation of Claims 5 and 15, namely, "the intervention circuit is instantiated such that the driver circuitry is between the intervention circuit and the wordline" (Specification page 14 lines 1-4 and 10-11; note that the intervention circuit is element 316, output node 306 couples to the actual wordline signal, and element 310 is a driver transistor pair).

The Applicants also respectfully traverse the objection to the Specification on page 4 of the Office Action. Specifically, "powering down, with a power switch,

the circuitry for operating the row of memory cells preceding the intervention circuit" is element 320 of FIG. 3 (Specification page 14 lines 18-20 and page 15 lines 6-8; see also element 118 of FIG. 1a plus page 11 lines 14-17 and page 12 lines 8-9). FIG. 3 also shows the limitation of Claims 5 and 15, namely, "the intervention circuit is instantiated such that the driver circuitry is between the intervention circuit and the wordline" (Specification page 14 lines 1-4 and 10-11; note that the intervention circuit is element 316, output node 306 couples to the actual wordline signal, and element 310 is a driver transistor pair).

Claim 1 positively recites operating the intervention circuit to retain the row of memory cells in a desired state, and powering down, with a power switch, the circuitry for operating the row of memory cells preceding the intervention circuit. In addition Claim 1 positively recites that the intervention circuit is operated by a first signal source, separate from a second signal source that powers down the circuitry for operating the row of memory cells preceding the intervention circuit. These advantageously claimed features are not taught or suggested by the patents granted to Itoh et al., Yanagisawa et al. or Akiba et al, or; either alone or in combination.

Itoh et al. does not teach the advantageously claimed invention because Itoh et al. does not teach a powering down step (column 6 lines 15, 23, and 55-62, FIGS. 7a-8f). The Applicants respectfully traverse the assertion in the Office

Action (page 5) that FIG. 7b of Itoh et al. shows a wordline driver; the Applicants submit that FIG. 7b is an address decode circuit (column 6 lines 9-11 and 28-29).

The Applicants respectfully traverse the characterization of Itoh et al.'s FIG. 4 in the Office Action (page 6). More specifically, the Applicants respectfully traverse the assertion that Q'9 is the intervention circuit and Q'6 is the power switch. The Applicants submit that Q'9 and Q'6 are the standard precharge and evaluation transistors of a dynamic logic gate. Q'6 does not turn off power – it is turned off during a portion of a cycle as a part of the dynamic logic gate function. In addition, Q'9 is not an intervention circuit. If the WL is low then Q'9 will keep P3 high against leakage currents (and thus keep WL low), but if the WL is high then it will not bring the WL low. Furthermore, Q'9 does not keep the WL low when the power is off. Q'9 keeps P3 high when Q'6 is off. Q'9 is gated by the WL and only has a role when Q'6 is on and Q'9 is off. Moreover, Q'6 and Q'9 are gated by the same signal, namely CE. When Q'6 is off, Q'9 is on and P3 is charged high. When Q'6 is turned on, Q'9 is turned off and P3 may or may not be discharged (depending on the other inputs).

Akiba et al. does not teach the advantageously claimed invention because Akiba et al. does not teach a powering down step (paragraphs 0086-0089). The Applicants respectfully traverse the assertion in the Office Action (page 8) that

FIG. 13 of Akiba et al. shows a wordline driver; the Applicants submit that FIG. 13 is an address decode circuit (paragraphs 0086 and 0089).

Yanagisawa et al. does not teach the advantageously claimed invention because Yanagisawa et al. does not teach a powering down step (page 8 paragraph 0111, FIG. 16B). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NOR gate high is not considered powering down the NOR gate. Moreover, there is a big difference between a power switch and a portion of a NAND gate or the NOR gate (FIG. 16B). Moreover, Yanagisawa does not teach and intervention circuit that is operated by a first signal source separate from a second signal source that powers down the circuitry for operating the row of memory cells preceding the intervention circuit, as advantageously claimed.

Regarding Claim 3, the Applicants respectfully traverse the statement in the Office Action (page 5) that "...it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well." The Applicants submit that transistors and resistors are not always interchangeable because transistors can be turned off and resistors cannot be turned off. The resistor only works in certain situations, such as the Applicants', where a high value resistor could be used to keep the wordline low in the sleep mode, yet have a weak enough pull down effect that the wordline could be raised by the

wordline driver in the active mode. The Applicants also traverse the assertion in the Office Action (pages 2-3) that the Applicants argued "in Applicants argument, page 11" an "advantage of resistors over transistors". The Applicants submit that they didn't state that resistors have an advantage over transistors (see 111 Amendment dated 12/22/2004; see also Specification, page 11 lines 9-11). Moreover, the fact that the Modern Dictionary of Electronics may state that transistors can be considered variable resistors whose resistance depends on the current applied to the gate does not mean that a resistor can always be substituted for a transistor. The Applicants submit that for any one gate condition the transistor could be replaced by a resistor (see Specification, page 11 lines 9-11), but when a variable gate voltage is applied the transistor cannot be replaced by a resistor.

Regarding Claim 6, the Applicants respectfully traverse the assertion in the Office Action (page 6) that element 71 is a driver circuit. The Applicants submit that element 71 is not a driver circuit and elements 74, 76 are the driver elements of the address decode circuit in FIG. 7b of Itoh et al.

Regarding Claim 23, the Applicants respectfully traverse the assertion in the Office Action (page 6) that elements 71 and 72 are not WL pre-drivers and they are not powered down. The Applicants submit that elements 71 and 72 of FIG. 7 are not powered down. (Note that elements 73 and 75 drive elements 74

and 76 respectively; however, elements 74 and 76 are address line drivers and not WL drivers.)

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over the patents granted to Itoh et al., Yanagisawa et al. and Akiba et al; either alone or in combination. Furthermore, Claims 2-9 and 23 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Claim 11 positively recites an intervention circuit adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down with a power switch. These advantageously claimed features are not taught or suggested by the patents granted to Itoh et al., Yanagisawa et al., or Akiba et al.; either alone or in combination.

Itoh et al. does not teach the advantageously claimed invention because Itoh et al. does not teach a powering down step (column 6 lines 15, 23, and 55-62, FIGS. 7a-8f). The Applicants respectfully traverse the assertion in the Office Action (page 5) that FIG. 7b of Itoh et al. shows a wordline driver; the Applicants submit that FIG. 7b is an address decode circuit (column 6 lines 9-11 and 28-29).

Similarly, Akiba et al. does not teach the advantageously claimed invention because Akiba et al. does not teach a powering down step (paragraphs 0086-0089). The Applicants respectfully traverse the assertion in the Office Action (page 8) that FIG. 13 of Akiba et al. shows a wordline driver; the Applicants submit that FIG. 13 is an address decode circuit (paragraphs 0086 and 0089).

Yanagisawa et al. does not teach the advantageously claimed invention because Yanagisawa et al. does not teach a powering down step (page 8 paragraph 0111, FIG. 16B). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NOR gate high is not considered powering down the NOR gate. Moreover, there is a big difference between a power switch and a portion of a NAND gate or the NOR gate (FIG. 16B).

Regarding Claim 13, the Applicants respectfully traverse the statement in the Office Action (page 5) that "...it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well." The Applicants submit that transistors and resistors are not always interchangeable because transistors can be turned off and resistors cannot be turned off. The resistor only works in certain situations, such as the Applicants',

where a high value resistor could be used to keep the wordline low in the sleep mode, yet have a weak enough pull down effect that the wordline could be raised by the wordline driver in the active mode. The Applicants also traverse the assertion in the Office Action (pages 2-3) that the Applicants argued "in Applicants argument, page 11" an "advantage of resistors over transistors". The Applicants submit that they didn't state that resistors have an advantage over transistors (see 111 Amendment dated 12/22/2004; see also Specification, page 11 lines 9-11). Moreover, the fact that the Modern Dictionary of Electronics may state that transistors can be considered as variable resistors whose resistance depends on the current applied to the gate; that does not mean that a resistor can always be substituted for a transistor. The Applicants submit that for any one gate condition the transistor could be replaced by a resistor (see Specification, page 11 lines 9-11), but when a variable gate voltage is applied the transistor cannot be replaced by a resistor.

Regarding Claim 16, the Applicants respectfully traverse the assertion in the Office Action (page 6) that element 71 is a driver circuit. The Applicants submit that element 71 is not a driver circuit and elements 74, 76 are the driver elements of the address decode circuit in FIG. 7b of Itoh et al.

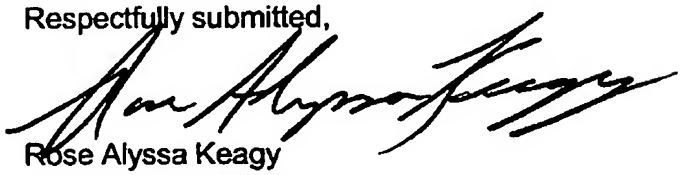
Regarding Claim 24, the Applicants respectfully traverse the assertion in the Office Action (page 6) that elements 71 and 72 are pre-drivers. The

Applicants submit that elements 71 and 72 of FIG. 7 are not WL pre-drivers and they are not powered down. (Note that elements 73 and 75 drive elements 74 and 76 respectively; however, elements 74 and 76 are address line drivers and not WL drivers.)

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 11 and respectfully assert that Claim 11 is patentable over the patents granted to Itoh et al., Yanagisawa et al. and Akita et al.; either alone or in combination. Furthermore, Claims 12-18 and 24 are allowable for depending on allowable independent Claim 11 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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